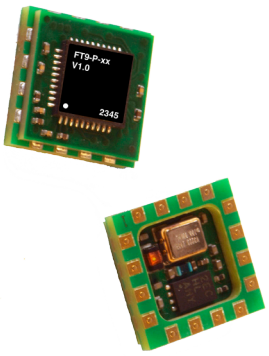
DATA SHEET

FT9-P
Jitter Attenuating Frequency translator

Overview



The FT9-P is a small, self-contained frequency translator and jitter attenuator designed to meet requirements for multiple applications where low phase noise and ultra-low jitter outputs are required including: frequency translation supporting wireless communication, 40G,100G and 400G Synchronous Ethernet, OTN and IEEE 1588 network elements, clock translation with low phase noise, and other applications demanding sub-picosecond jitter performance.

The FT9-P consists of a PLL stage that attenuates the jitter of the reference input with the use of an integrated phase detector, charge pump and internal VCXO. The FT9-P generates a single-ended LVCMOS 3.3V clock output based on the frequency of the internal VCXO chosen. The FT9-P accepts one reference input from 8kHz to 125MHz, also at a +3.3V LVCMOS level. The FT9-P can be configured with an internal LVCMOS VCXO from 10MHz to 160MHz. The internal disciplined VCXO provides the output characteristics for phase noise and jitter performance for the clock output, which can be further divided down at the output port with 6-bit divider value achieving output frequencies as low as 156.25kHz. This product is based on Connor-Winfield's NF1011 frequency translating IC and is intended to be provided as a factory configured and programmed module for the ease of use and convenience of the user.

Features

- Phase locks to an incoming reference input from 8 kHz to 125MHz
- Generates a single ended Low Jitter Clock Outputs derived from its internal VCXO
- Status indicators for phase-lock verification and loss of signal (LOS) notification.
- Internal VCXO supports up to 156.25 MHz clock output frequency range
- 3.3VDC Supply Voltage
- -40°C to 105°C operating temperature range
- 9.2 x 9.2mm 16 pin QFN surface mount package

Applications

- High Stability Clocking
- Primary Reference Time Clock (PRTC) [G.8272]
- Telecom Grand Master [G.8273.1]
- Telecom boundary clock [G.8273.2]
- Wireless Base Stations
- GNSS Disciplined Oscillator
- NTP Stratum 0 Standard

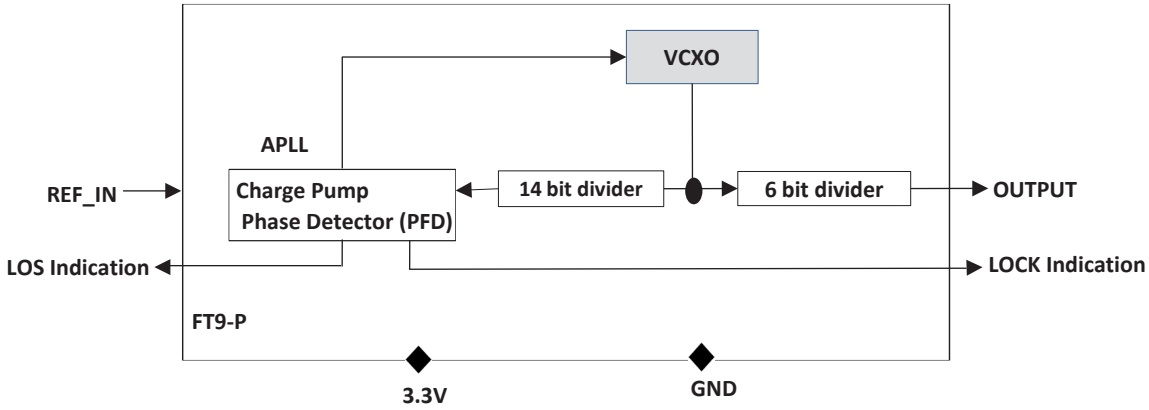
General Description

The FT9-P module is designed to receive a 3.3V Reference input and generate a frequency-translated single-ended clock output phase locked to the incoming reference input signal.

The PLL consists of an integrated charge pump and phase detector, which locks to an on-board VCXO. The module translates the reference input frequency and attenuates the jitter on the incoming clock signal. The internal VCXO on the FT9-P module provides the output characteristics for phase noise and jitter performance for the clock output.

This module is configured at the factory based on the internal VCXO frequency chosen and requires no additional external components for operation. The model number is configured with an input frequency designator and an output frequency designator.

FT9-P Functional Block Diagram



Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Power Supply Voltage (Vdd)	-0.3	-	4.0	Volts	
Storage Temperature	-55	-	125	°C	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Input Frequencies	8k	-	125.0 M	Hz	
Output Frequencies	156.25k	-	156.25 M	Hz	
Supply Voltage (Vdd)	3.13	3.3	3.46	Volts	
Supply Current	-	80	100	mA	
REF_IN Voltage	2.7	-	3.3	Vpp	
Operating Temperature	-40	-	105	°C	
SSB Phase Noise for FT9-P-AB					
at 10Hz offset	-	-57	-	dBc/Hz	
at 100Hz offset	-	-92	-	dBc/Hz	
at 1kHz offset	-	-128	-	dBc/Hz	
at 10kHz offset	-	-138	-	dBc/Hz	
at 100kHz offset	-	-150	-	dBc/Hz	
at 1MHz offset	-	-155	-	dBc/Hz	
at 10MHz offset	-	-155	-	dBc/Hz	

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Output Voltage					
(High) (Voh)	3.0	-	-	V	
(Low) (Vol)	-	-	0.4		
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	-	6	ns	

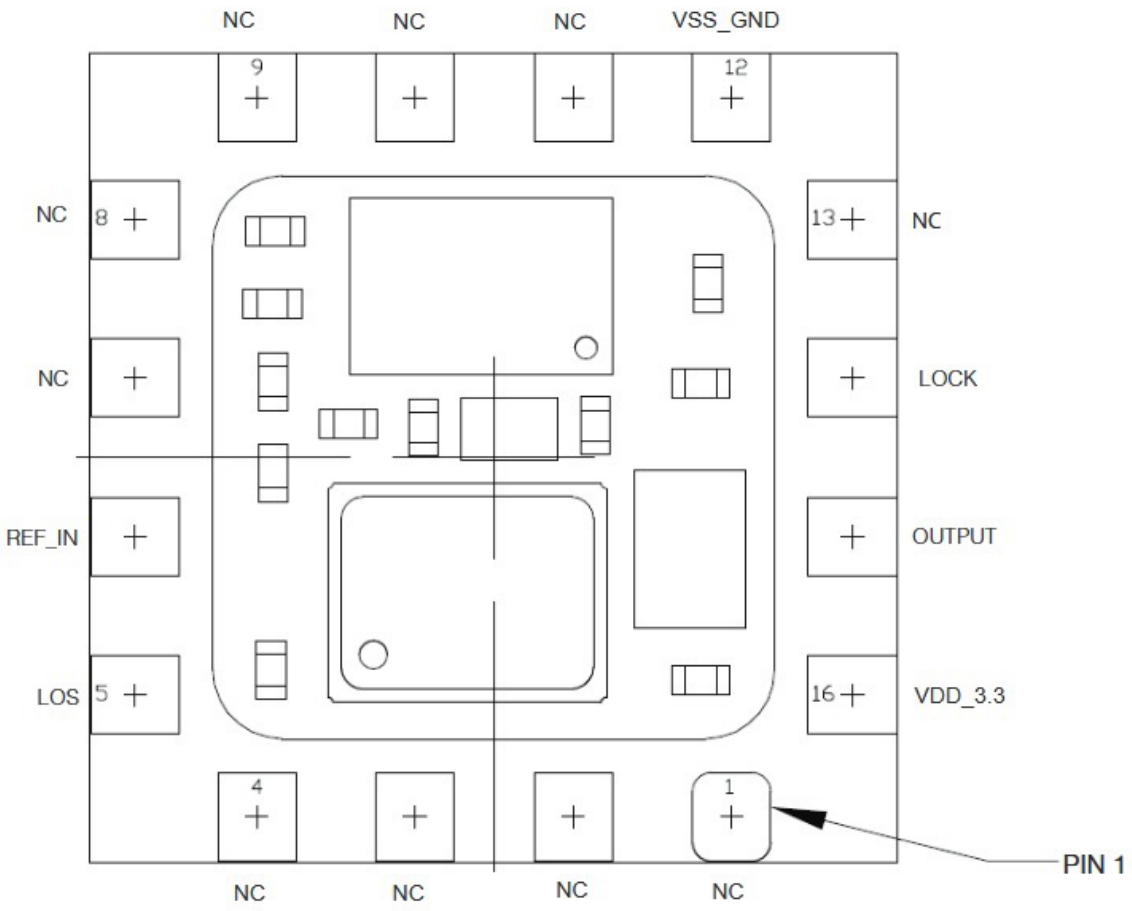
Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock:	Mechanical Shock per MIL Std 883E Method 2002.4 Test Condition B
Soldering:	SMD product suitable for Convention Reflow soldering. Peak temperature 260°C. Maximum time above 220°C, 60 seconds.
Solderability	Solderability per Mlil Std 883E Method 2003. See Solder Profile on Page 4.

Package Characteristics

Package	9.2 x 9.2mm 16 pin QFN
Moisture Sensitivity Level	MSL-3

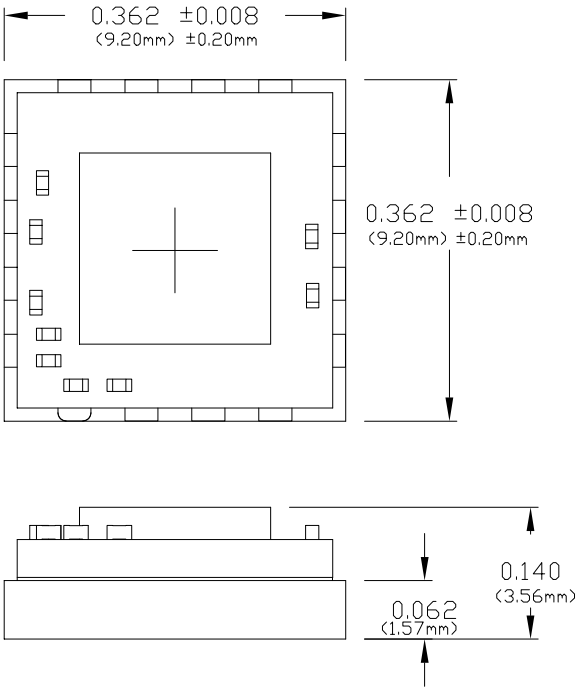
FT9-P Pin Assignments (Bottom View)

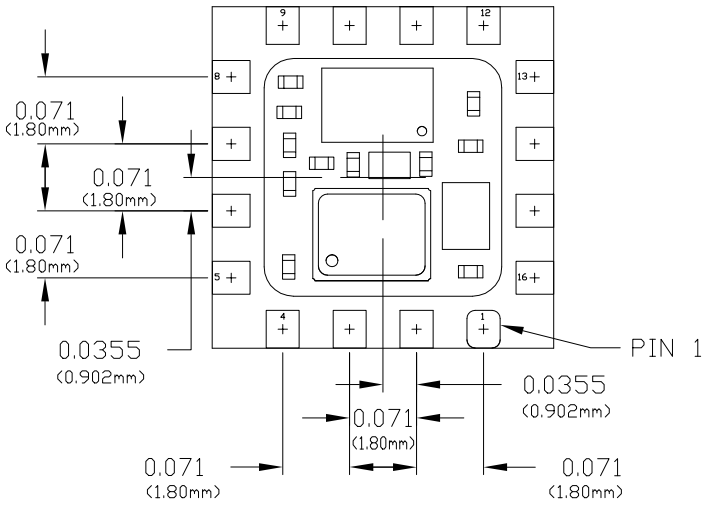


FT9-P Pin Description

Pin No.	Pin Name	I/O	Description
1	NC		
2	NC		
3	NC		
4	NC		
5	LOS	O	Loss of signal when pin goes HIGH, reference is present when pin is LOW
6	REF_IN	I	Reference input. Accepts 3.3V LVCMOS clock signal input
7	NC		
8	NC		
9	NC		
10	NC		
11	NC		
12	VSS_GND	Power	GROUND
13	NC		
14	LOCK	O	Lock indication when pin goes HIGH, not locked when pin is LOW
15	OUTPUT	O	3.3V LVCMOS Output
16	VDD_3.3	Power	3.3V Power Input

FT9-P Mechanical Drawing

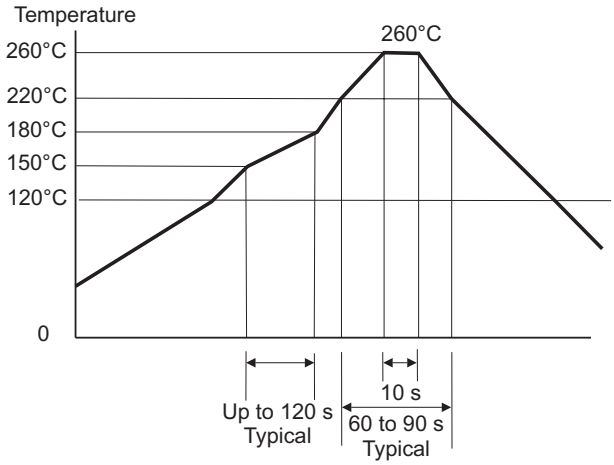




(BOTTOM VIEW)

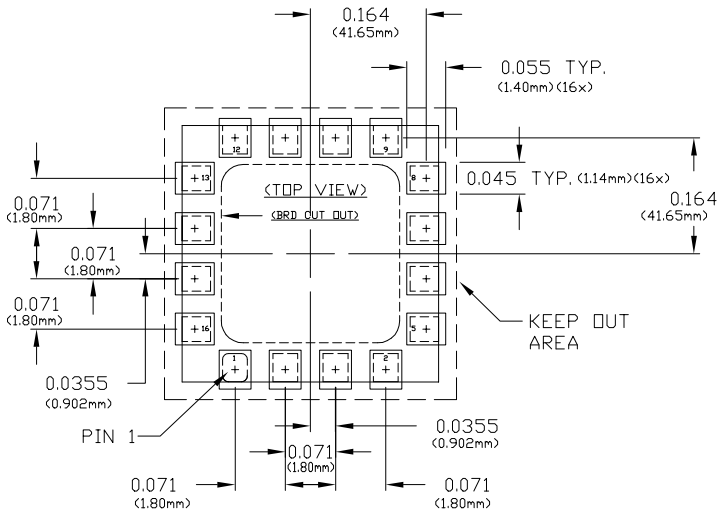
Dimensional Tolerance:
±0.005 (±0.127mm) unless shown otherwise

Solder Profile



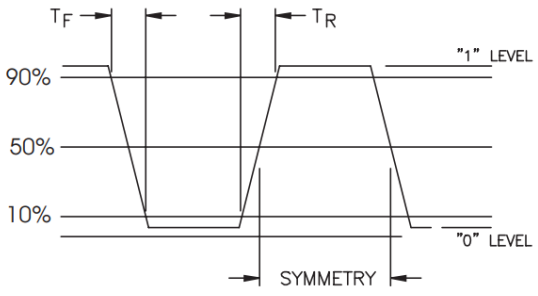
Meets IPC/JEDEC J-STD-020C

Suggested Pad Layout



KEEP OUT AREA
UNDER THE PCBOARD IS A KEEP OUT AREA,
DO NOT PLACE ANY PARTS IN THIS AREA.

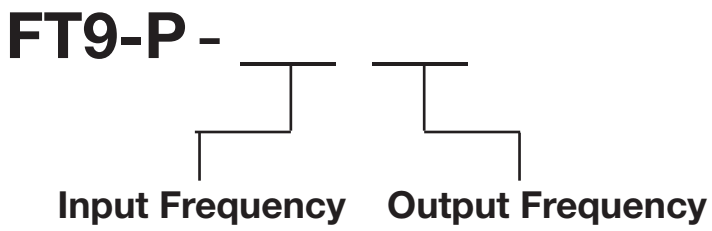
Output Waveform



Standard Frequencies

10.0 MHz	A		
100.0 MHz	B	65.536 MHz	T
122.88 MHz	C	32.768 MHz	W
125.0 MHz	D	64.0 MHz	X
156.25 MHz	E	38.88 MHz	Y
80.0 MHz	F	51.84 MHz	Z
98.304 MHz	G		
61.44 MHz	H	16.384 MHz	0
77.76 MHz	J	30.72 MHz	1
155.52 MHz	K	20.48 MHz	2
50.0 MHz	L	5.0 MHz	3
64.0 MHz	M	12.8 MHz	4
40.0 MHz	N	49.152 MHz	5
20.0 MHz	O	16.0 MHz	6
25.0 MHz	P	19.44 MHz	7
96.0 MHz	R	10.24 MHz	8
81.92 MHz	S	8 kHz	9

Ordering Information
(see standard frequencies listed above)



Example Part Number: FT9-P-AC

Input Frequency: 10.0 MHz
Output Frequency: 122.88 MHz

Revision History

Revision	Date	Note
00	09/13/23	New Release
01	12/28/23	Update photo image, add marking configuration
02	12/12/24	Update page 3 pin assignments image to agree with pin description table
03	04/22/24	Update the Supply Current parameter

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