Integrated IC Solutions for the Synchronous Timing Source in Network Elements

NS3D02 APLL Circuit Design Guide and Simulation Notes and Download Tool

Application Note 09

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1. Overview of the NS3D02 APLL Circuit

The NS3D02 includes an integrated APLL (Analog Phase-Locked Loop) block designed to operate with an external VCXO. It enables low-jitter, high-stability clock synthesis for timing-critical applications. This analog loop uses a charge pump and a passive loop filter to dynamically control the VCXO.

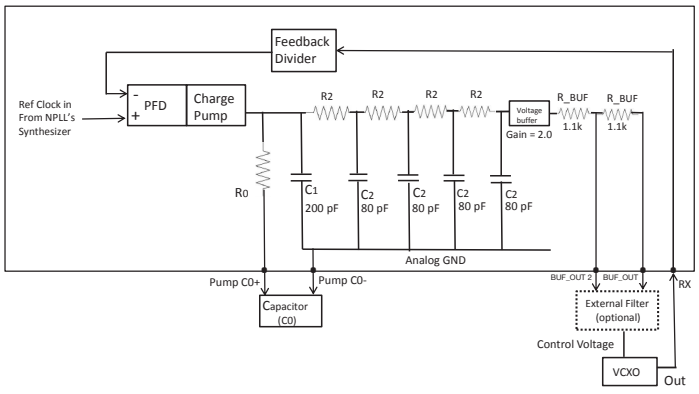
2. APLL Circuit Schematic (from NS3D02 Datasheet, Page 11)

Below is the exact analog PLL configuration as documented in the NS3D02 datasheet on page 11 under the 'APLL Configuration' section.

APLL Configuration

The analog PLL (APLL)'s function in NS3D02 is to discipline the external VCXO to output up to two divided down clocks. The APLL will take a clock synthesized by the NPLL as its reference input, translate the frequency to higher frequency and also attenuate the jitter generated by NPLL's digital clock synthesizer.

NS3D02's APLL circuit contains a phase frequency detector (PFD), a programmable charge pump, an uncompleted programmable passive low-pass filter (LPF), a fixed-gain voltage buffer, and a programmable clock feedback divider. With some extra external capacitors to complete the LPF, the APLL can operate to cover loop bandwidth ranging from 10Hz to 200 Hz easily.



3. How the APLL Works

The Analog Phase-Locked Loop (APLL) inside the NS3D02 works by comparing a reference frequency to a divided-down version of the VCXO output and using the phase error to adjust the VCXO frequency. Here is a step-by-step breakdown:

- A reference clock drives the Phase Frequency Detector (PFD).
- The PFD compares the phase of the reference and the feedback from the VCXO.
- It generates UP/DOWN pulses to a programmable charge pump.
- The charge pump outputs a current proportional to phase error.
- An external passive loop filter (R0, C0, R2, C2) converts current to voltage.
- A voltage buffer amplifies the control voltage and drives the VCXO.
- The VCXO adjusts frequency to maintain phase lock.

4. Theory of the NS3D02 APLL Loop Filter Architecture

The APLL loop filter in the NS3D02 is implemented as a **seond-order passive low-pass filte**r, critical for stabilizing the phase-locked loop and shaping the dynamic response. In this architecture:

- **C0** is the **only external filter component**. It is connected to the PUMP_C+ and PUMP_C– pins and sets the primary integrator's capacitance.
- **R0 and R2** are **internal programmable resistors** selected via device registers. These resistors define the frequency poles and zero of the loop filter.
- **C1 and C2** are **fixed internal capacitors**, not configurable, which act in conjunction with R0 and R2 to form the full loop response.
- The **voltage buffer output** includes fixed **internal series resistors** (typically 1.1 kΩ) at BUF_OUT and BUF_OUT2, which influence post-filtering if external RC components are used.

This hybrid filter configuration allows the loop dynamics to be tailored via register settings, with **only one capacitor (C0)** needed externally. This reduces design complexity and board footprint while maintaining tuning flexibility.

The **primary loop bandwidth**, damping factor, and phase margin are influenced by:

- The value of external **C0**
- The selected internal **R0 and R2** settings (via registers)
- The **charge pump current** setting (also register-controlled)
- The **VCXO tuning gain (Kv)** in ppm/V

Author:
Engineering Support
9Co

2111 Comprehensive Drive | Aurora, Illinois 60505
Phone: 630-697-2336 | Email: info@9co.com | www.9co.com

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5. Recommended External Component Values

The NS3D02 APLL circuit is designed with a mostly integrated loop filter architecture. Only one component, C0, is required externally, while the remaining loop filter elements are internal to the IC and configured through registers.

External Capacitor (C0):

This is the primary component determining the loop filter's integration behavior. It connects to the PUMP_C+ and PUMP_C– pins. Typical values range from **10 nF to 220 nF**, depending on the desired loop bandwidth and VCXO tuning characteristics. Use a **C0G/NP0 ceramic capacitor** for best thermal and electrical stability. Avoid high-k ceramics (X7R/X5R) as they introduce temperature-dependent drift and dielectric absorption.

Internal Components (Configured via Registers):

- **R0**: Sets the primary resistance in the integrator stage. Selectable through APLL_R0_VALUE_L/S registers.
- **R2**: Sets the zero location in the loop transfer function. Configurable through APLL_R2_DIV.
- **C1 and C2**: Internal fixed-value capacitors matched to the internal filter topology.
- **CP Current**: The loop gain is further shaped by the charge pump current, set using the APLL_CP_CURRENT register.

VCXO Selection:

The VCXO's tuning sensitivity (Kv) is a critical loop parameter. Most VCXOs operate in the 1**0–100 ppm/V** range. For low-jitter applications or tight holdover performance, use VCXOs with well-documented linear tuning characteristics. OCVCXOs may have lower pull ranges (e.g., 1–10 ppm/V) and may require narrower loop bandwidths to avoid instability.

Optional Post-Buffer RC Filter:

If needed, add a passive RC filter between BUF_OUT and the VCXO control input to suppress high-frequency ripple. This is especially helpful in noisy environments or with high-gain VCXOs. Use:

- **R = 1–10 kΩ** (metal film)
- **C = 10–100 nF** (C0G/NP0), placed close to the VCXO

This RC network is optional and should be validated by jitter performance measurements in the target application.

Design Insight:

Because the majority of the loop filter is internal and register-configurable, designers can use software tools or spreadsheets to simulate loop behavior based on register settings, external C0, VCXO characteristics, and desired phase margin.

Download Calculation and Simulation tool HERE:

6. VCXO Control Interface and Optional External Filter

The NS3D02 provides two output pins from its internal voltage buffer: BUF_OUT and BUF_OUT2. These outputs carry the control voltage derived from the loop filter and are designed to drive the control input of an external VCXO. However, to further suppress ripple or charge pump noise, an optional RC low-pass filter is often recommended between BUF_OUT and the VCXO control input.

A typical configuration includes a series resistor (1–10 kΩ) and a capacitor (10–100 nF) to ground placed near the VCXO. BUF_OUT should be connected through this RC network to the VCXO control pin. BUF_OUT2 may be left floating, used for monitoring, or used to sink noise with a standalone capacitor to ground. Avoid tying both BUF_OUT and BUF_OUT2 directly together at the same node.

This additional filtering helps reduce high-frequency noise while preserving loop dynamics and overall stability. The goal is to ensure that VCXO control voltage is stable and clean, particularly in noise-sensitive applications such as timing and communications systems.

7. Noise and Layout Considerations

- Place bypass capacitors as close as possible to VCXO and APLL power pins.
- Use a continuous ground plane underneath the loop filter and VCXO.
- Route the VCXO control voltage trace away from switching signals.
- Consider shielding the control trace if board noise is a concern.
- Use a ferrite bead or small resistor in series with VCXO VDD to suppress high-frequency noise.

8. Summary

The NS3D02 APLL architecture offers excellent flexibility for analog frequency synthesis with a VCXO. By carefully selecting the external capacitor, tuning register settings, optimizing layout, and using adequate bypassing, designers can achieve tight lock performance, excellent phase noise, and low jitter.

1. The reference clock feeds into the Phase Frequency Detector (PFD).
2. The PFD compares the reference phase with the divided VCXO output.
3. It generates UP or DOWN signals based on the phase difference.
4. A programmable charge pump converts these signals into current pulses.
5. This current is filtered by a hybrid loop filter consisting of:
   - an external capacitor (C0)
   - internal programmable resistors (R0 and R2)
   - fixed internal capacitors (C1 and C2)
6. The filtered voltage is amplified by an internal voltage buffer with gain = 2.
7. The buffered output drives the VCXO's control voltage input, closing the feedback loop.